# NoC Symbiosis

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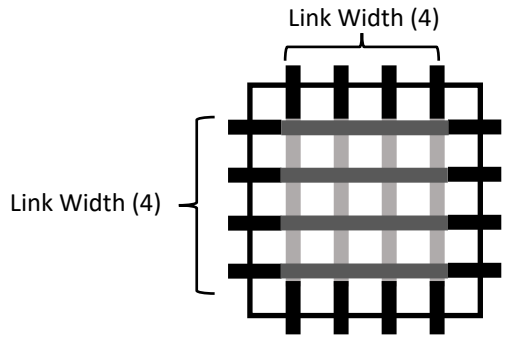
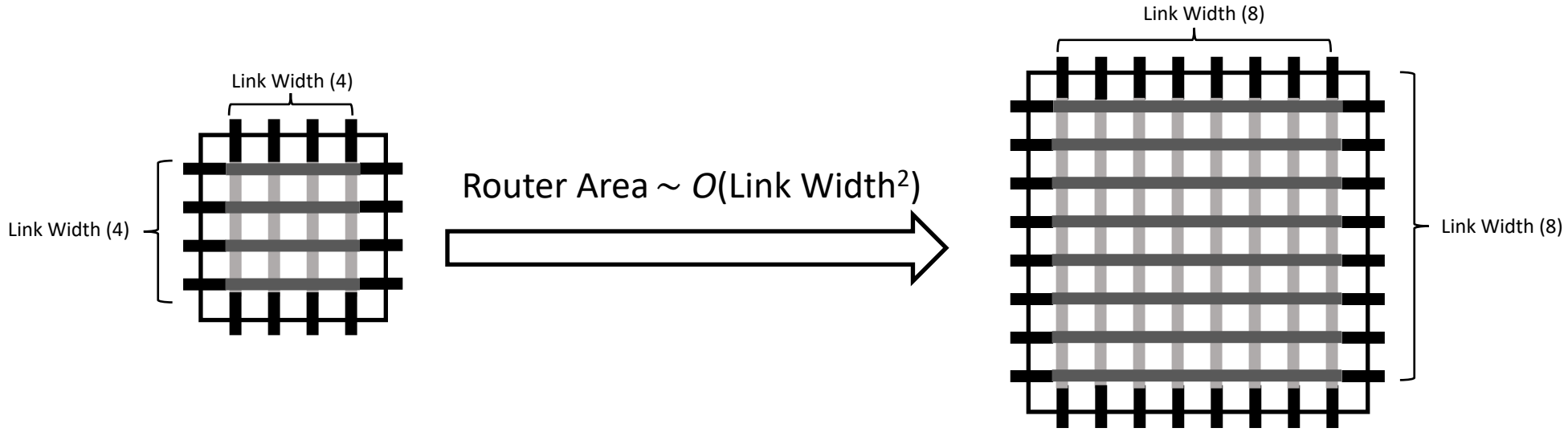
# Modeling a 2D Mesh Router




Link Width = 1X
Router Area = 1X

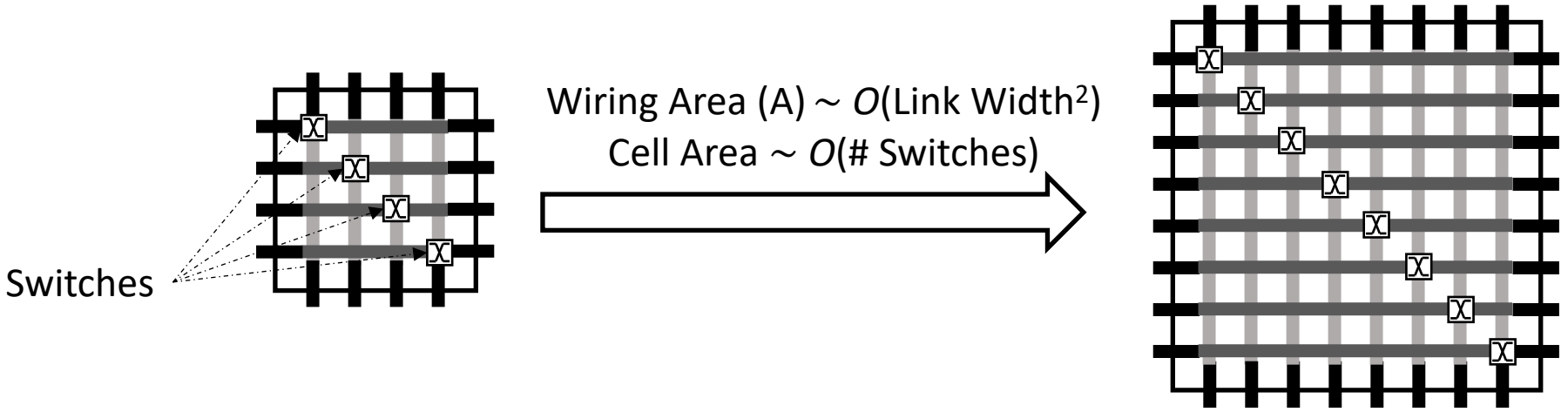
# Conventional Wisdom: Router Area Grows Quadratically With Link Width




Link Width = 1X
Router Area = 1X

Link Width = 2X
Router Area = 4X (Quadratic)

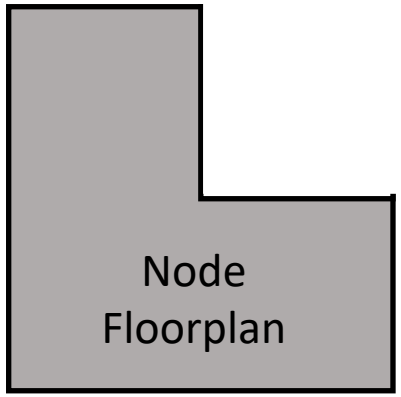
# Wiring Area Scales Quadratically and Cell Area Scales Linearly



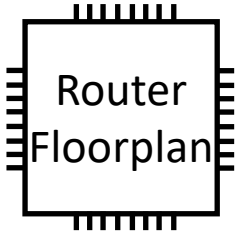

Link Width = 1X
Wiring Area = 1X
Cell Area = 1X

Link Width = 2X
Wiring Area = 4X (Quadratic)
Cell Area = 2X (Linear)

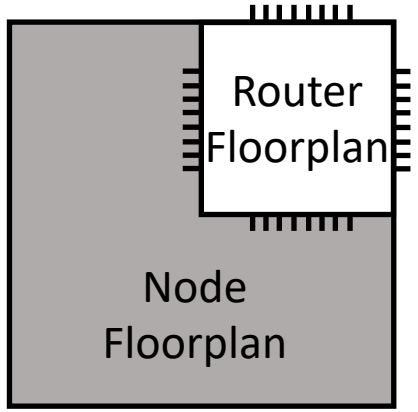
# Conventional Design Practices
# Consider the NoC and Node in Isolation




Step 1: Design Node Logic
(Accelerator, Processor, etc)

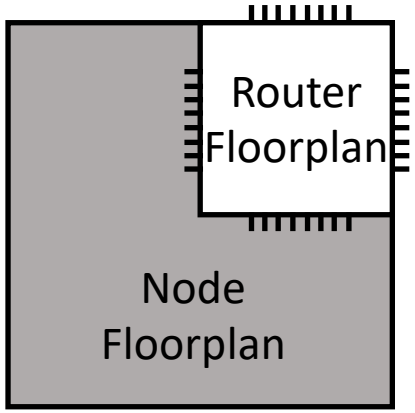



Step 2: Design NoC

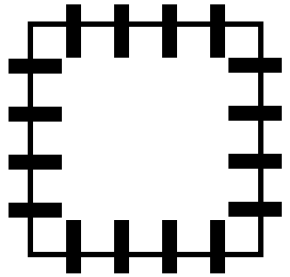



Step 3: Integrate

# The Divergence of Wire and Logic Resources Forces Designers to Choose the Lesser of Two Evils

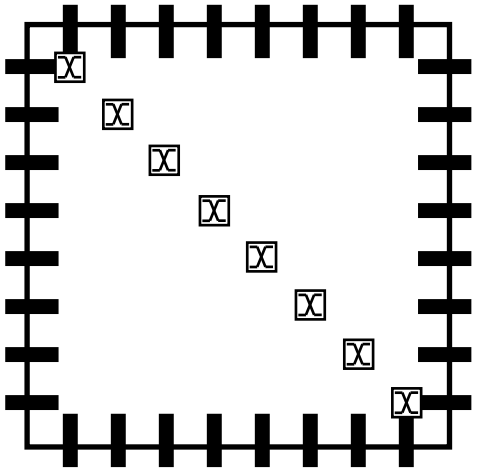



Balance Router Cell & Wiring Area



High Cell Area Utilization
Low Bandwidth

Large Network Links



Poor Cell Area Utilization
High Bandwidth

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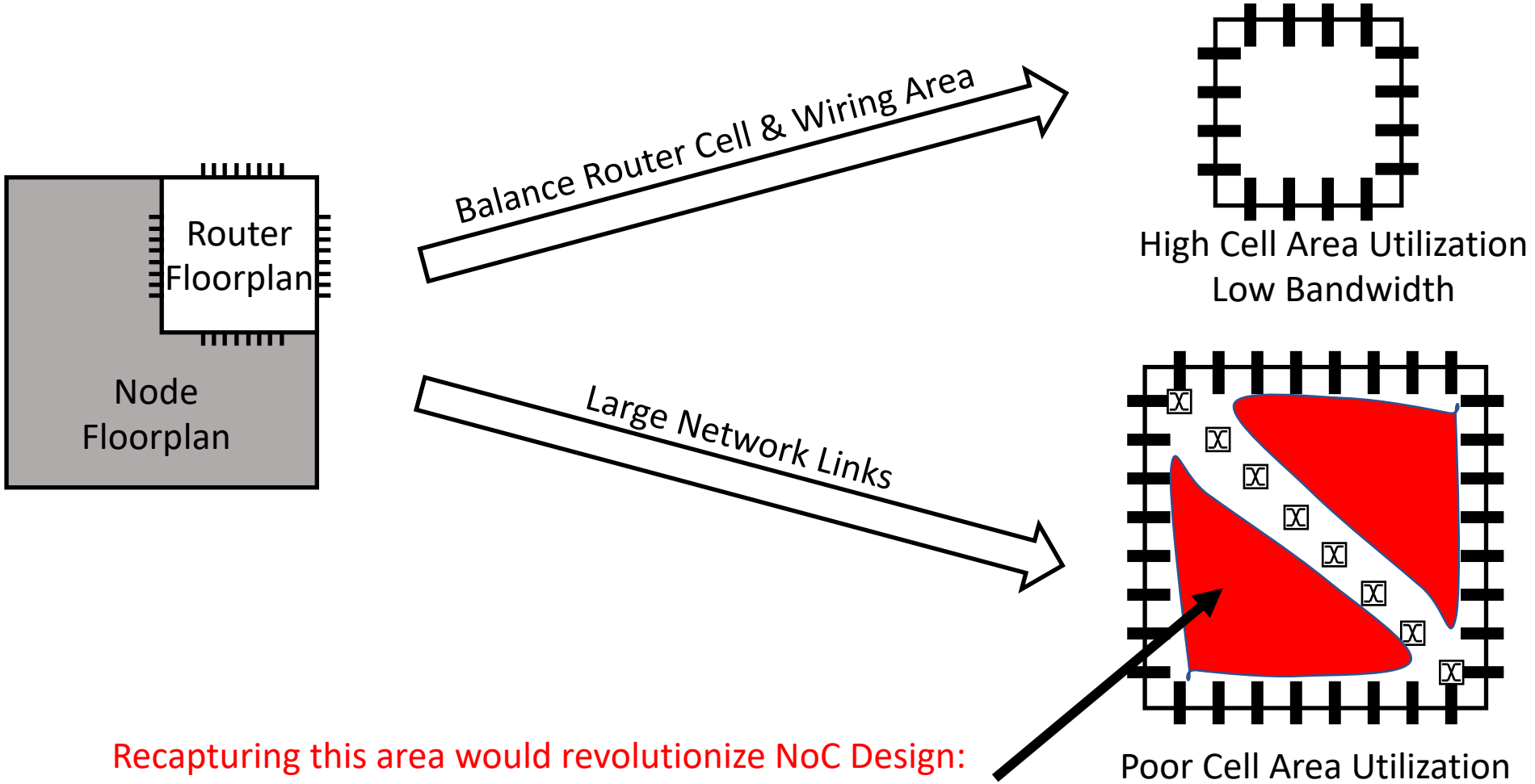
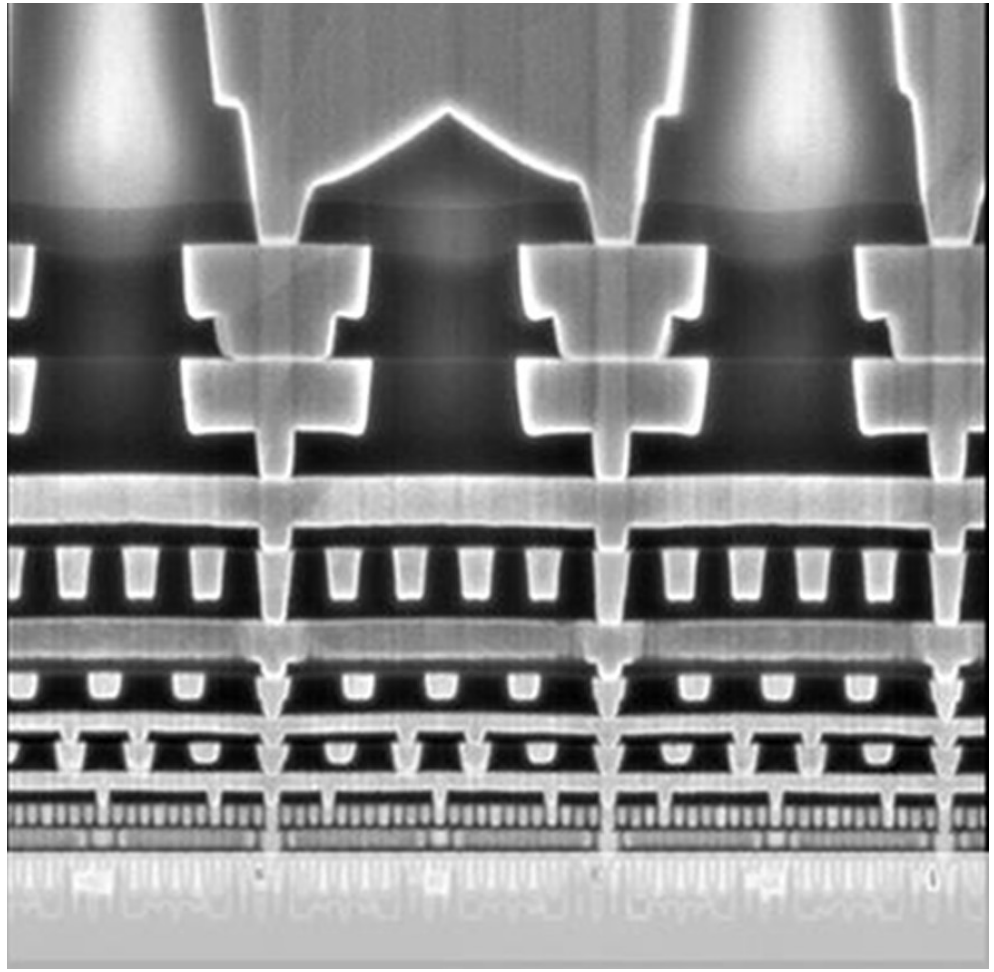


# Key Idea: Interconnect Utilization



(Intel, IEDM 2017)

**Interconnection Purpose**

Power Grid

Long-distance routing Wires

Logic Area and Local Routing

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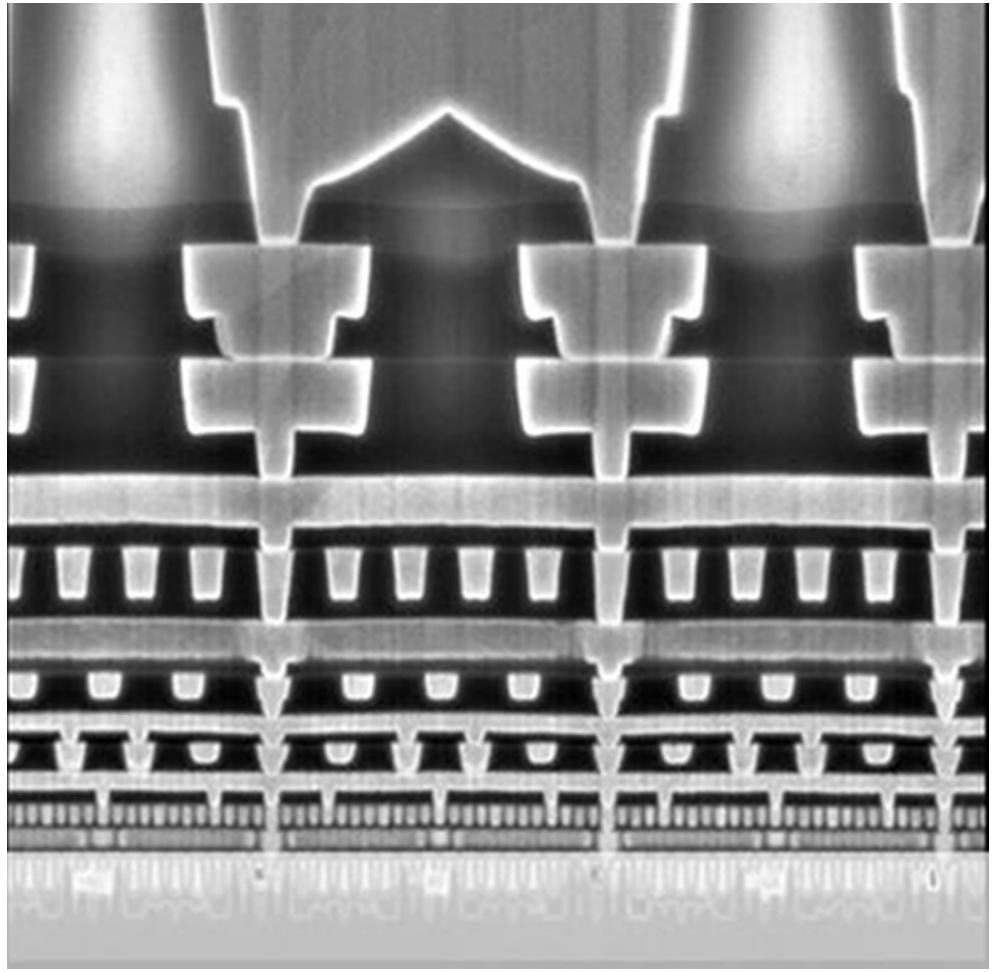
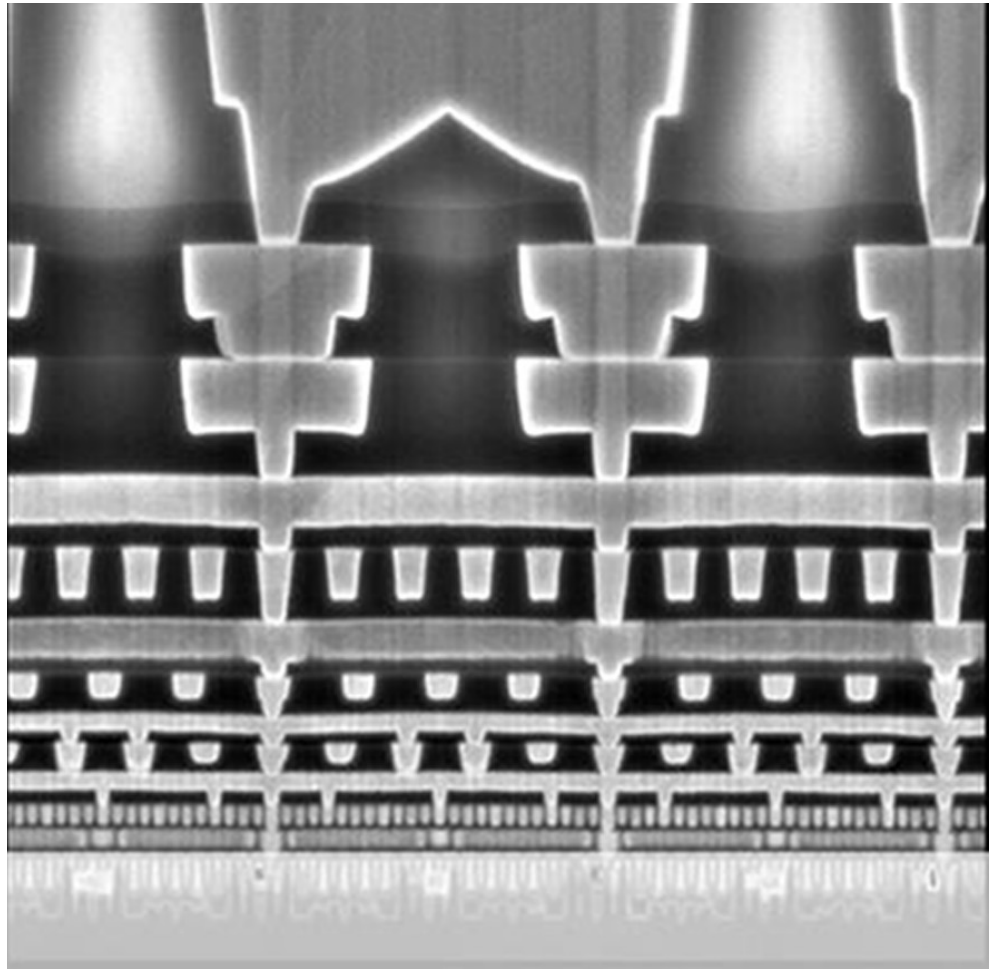


(Intel, IEDM 2017)

| Interconnection Purpose | Utilization | |
|---|---|---|
| | **Node** | **NoC** |
| Power Grid | | |
| Long-distance routing Wires | | |
| Logic Area and Local Routing | | |

# Key Idea: Interconnect Utilization



(Intel, IEDM 2017)

| Interconnection Purpose | Utilization | |
|---|---|---|
| | **Node** | **NoC** |
| Power Grid | | |
| Long-distance routing Wires | Low | |
| Logic Area and Local Routing | High | |

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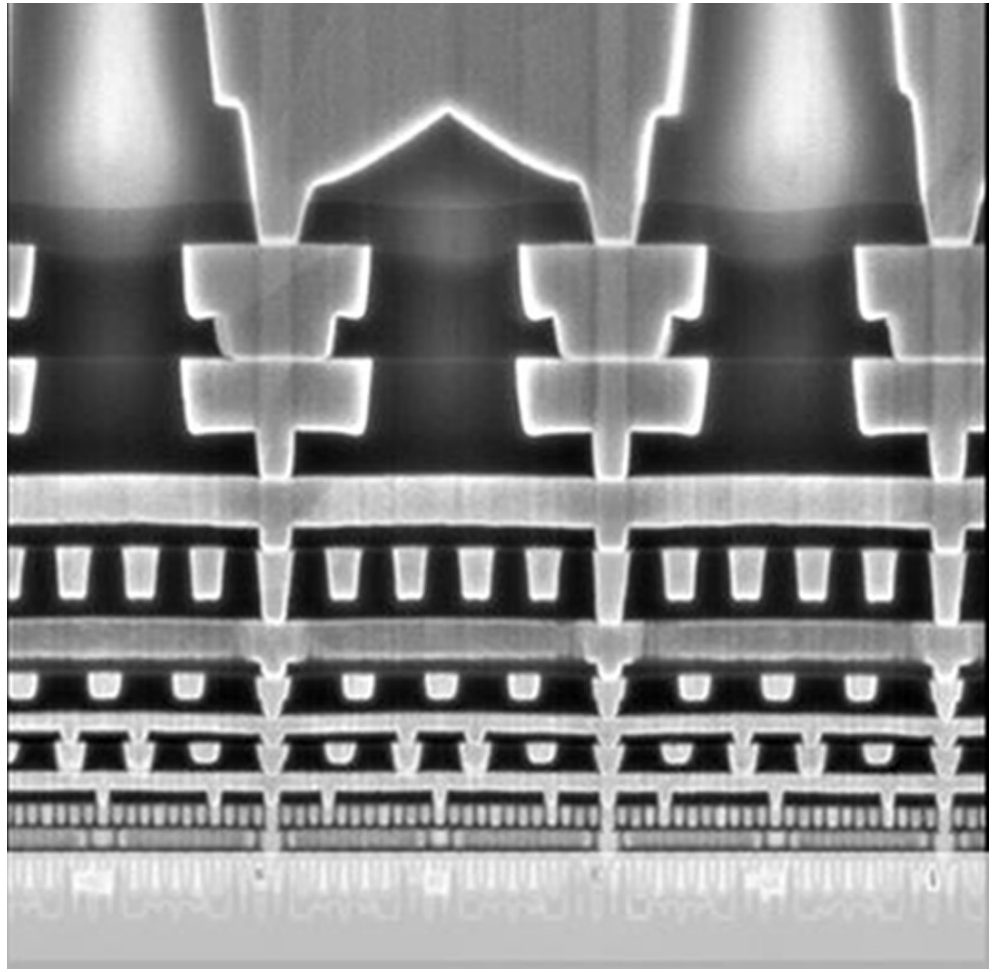
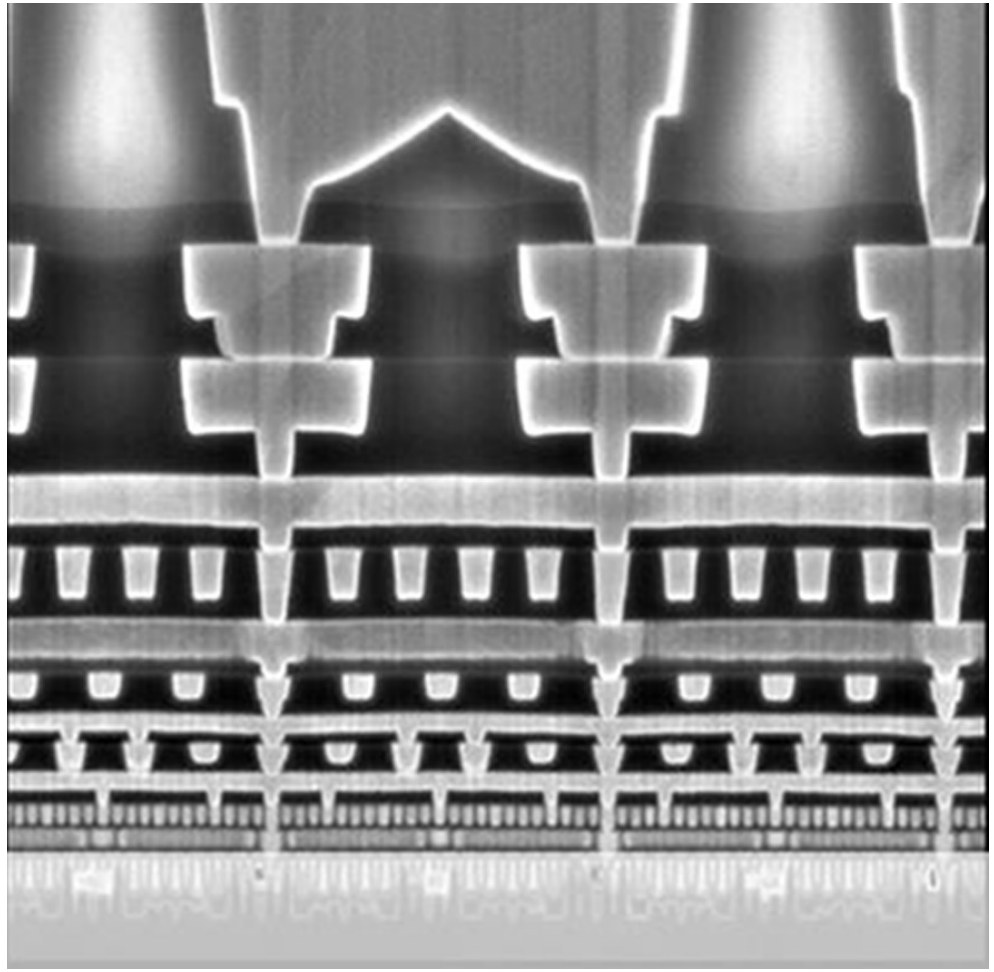


(Intel, IEDM 2017)

| Interconnection Purpose | Utilization | |
|---|---|---|
| | Node | NoC |
| Power Grid | | |
| Long-distance routing Wires | Low | High |
| Logic Area and Local Routing | High | Low |

# Node and NoC use *Complementary* Layers



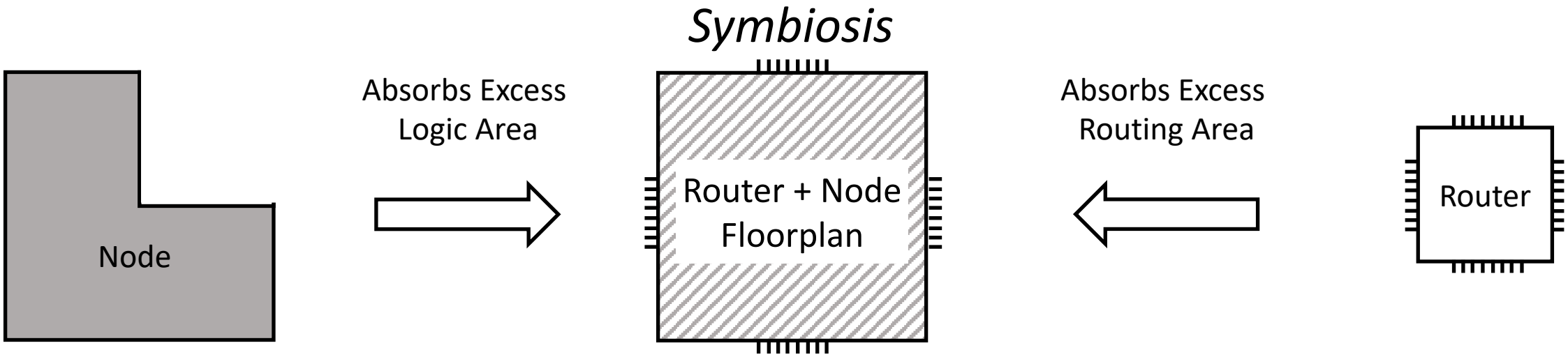
(Intel, IEDM 2017)

**Interconnection Purpose**

**Utilization**

| | Node | NoC | Combined |
|---|---|---|---|
| Power Grid | | | |
| Long-distance routing Wires | Low | High | High |
| Logic Area and Local Routing | High | Low | High |

# NoC Symbiosis Combines Router and Node Floorplans



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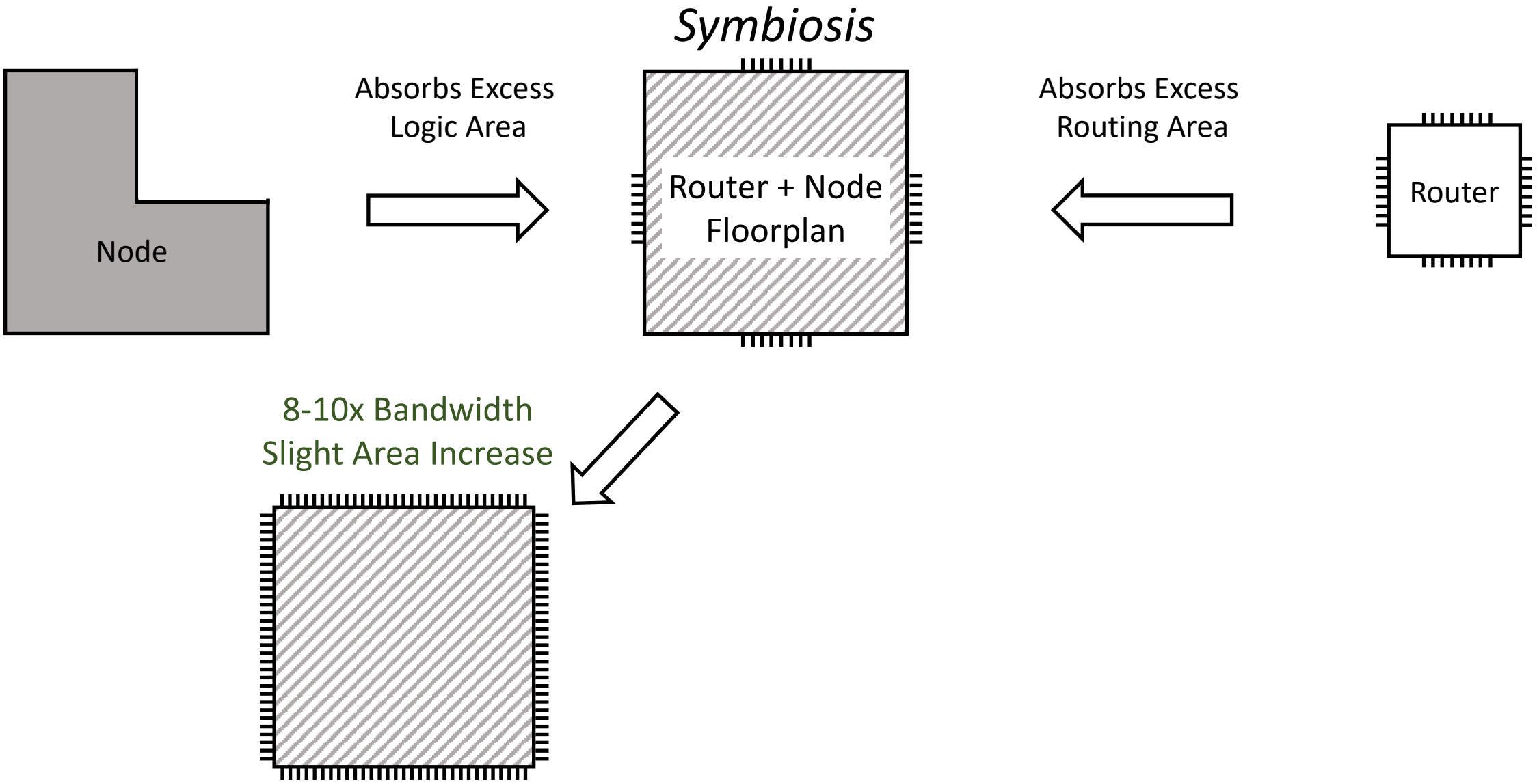

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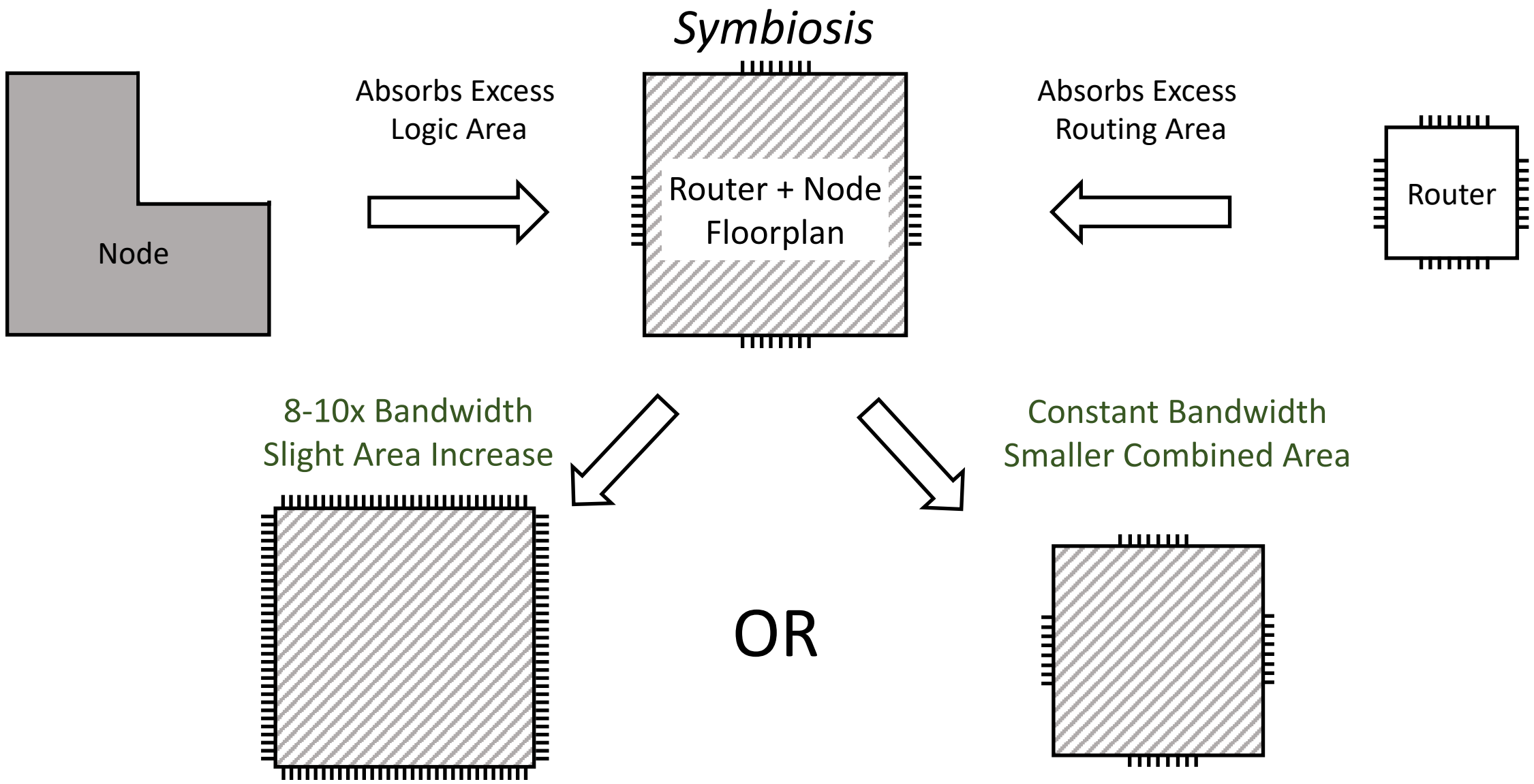
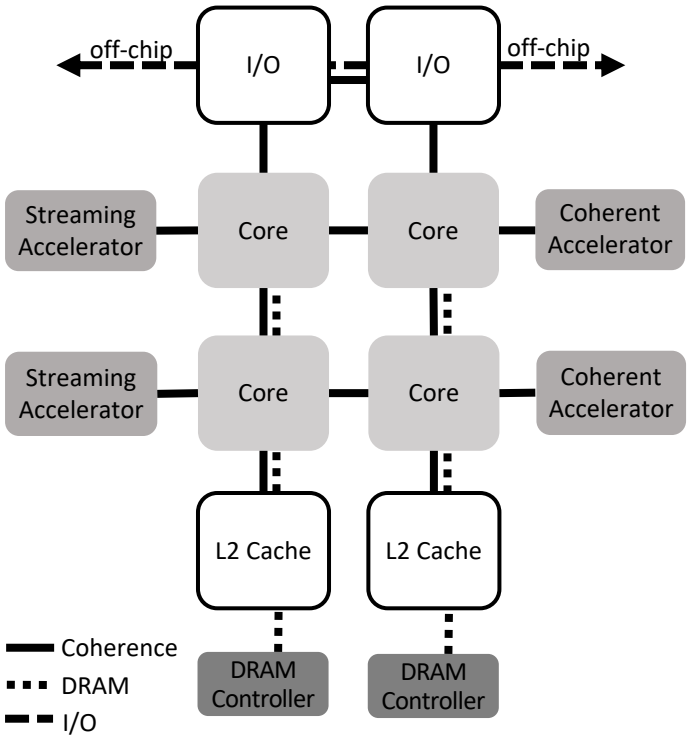


# Discovering Symbiosis with BlackParrot

- BlackParrot is an open source tiled, Linux-capable RISC-V coherent multicore
  - NoCs for coherence, memory and I/O
- BlackParrot is designed as a “base class” for the next generation of accelerator-based SOCs
- Join us! Fork, Clone, Contribute! github.com/black-parrot/black-parrot



# Once Upon A Time…

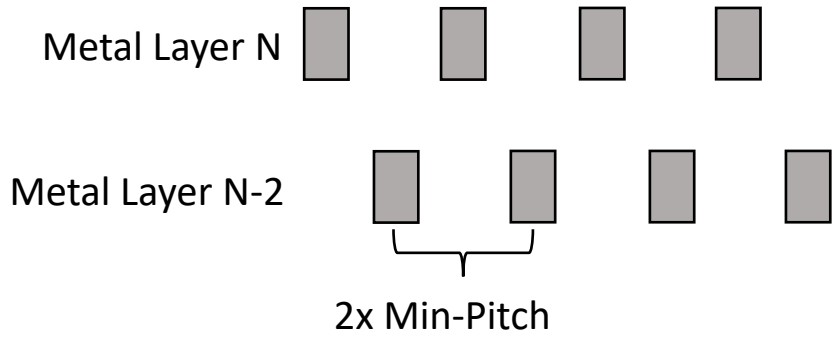
# Examining the Science of NoC Symbiosis

- At what link widths does NoC Symbiosis offer benefits?
- How effective are CAD tools at automatically exploiting NoC Symbiosis?
- What are the quantitative benefits of NoC Symbiosis?
- To what extent did prior chip designs leverage NoC Symbiosis?

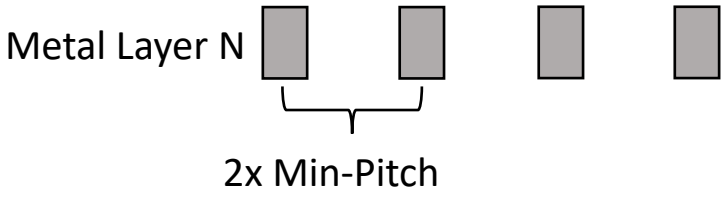
# NoC Symbiosis Experiments

- Network Configuration[1]
  - 2D Mesh Wiring
  - Dimension Ordered Routing
  - Wormhole Links
- Parameters:
  - Link Width
  - Pitch/Process Constraints (DLDT/SLDT)
- Measurements:
  - Total Router Area
  - Standard Cell Area
  - % Utilization (Cell / Router Area)
  - Maximum Bandwidth
- All Data in this Talk is Using Full Synthesis and APR of actual NoC designs in 12nm

Double-Layer Double Track (DLDT)



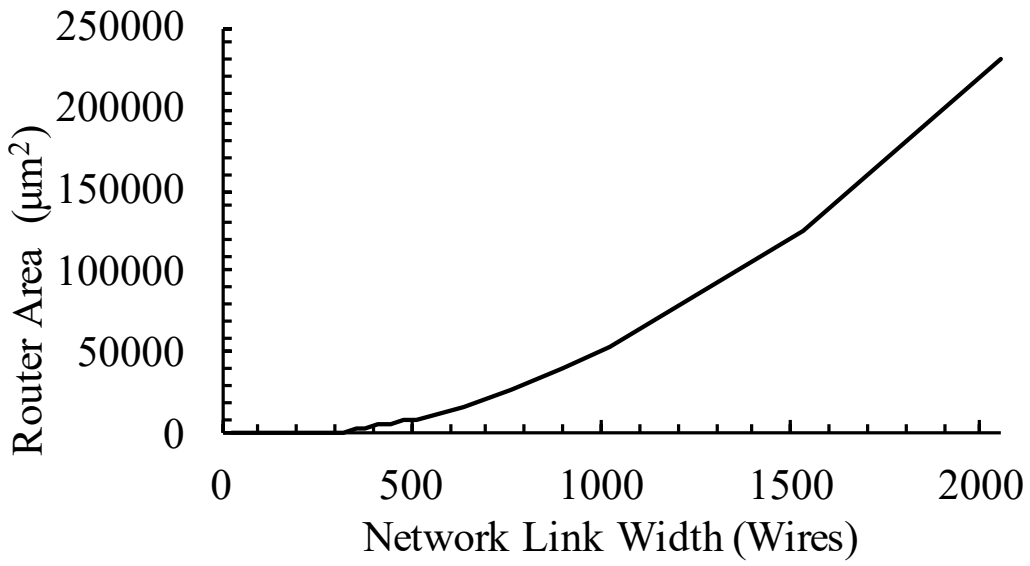

Single-Layer Double Track (SLDT)



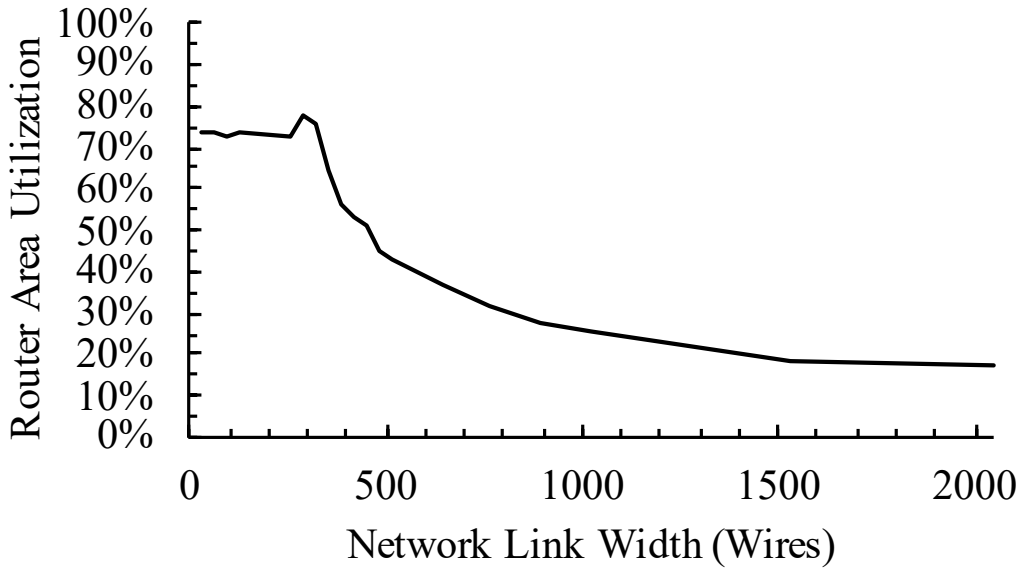

1: https://github.com/bespoke-silicon-group/basejump_stl/blob/master/bsg_noc/bsg_wormhole_router.v

# When does NoC Symbiosis Offer Benefits?

**Router Area vs Link Width**

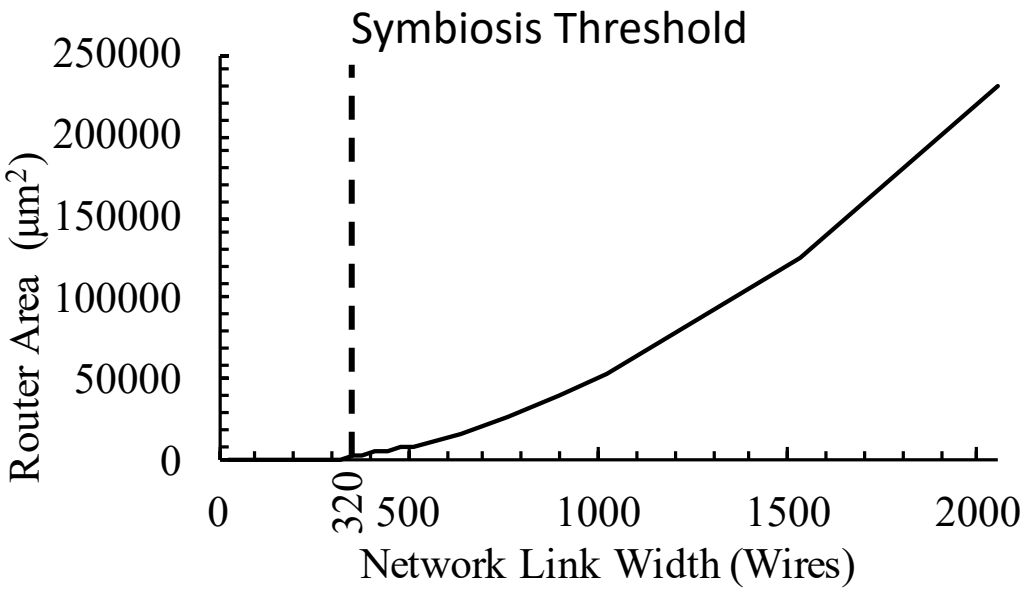



**Area Utilization vs Link Width**



# Above the NoC Symbiosis Threshold

**Router Area vs Link Width**

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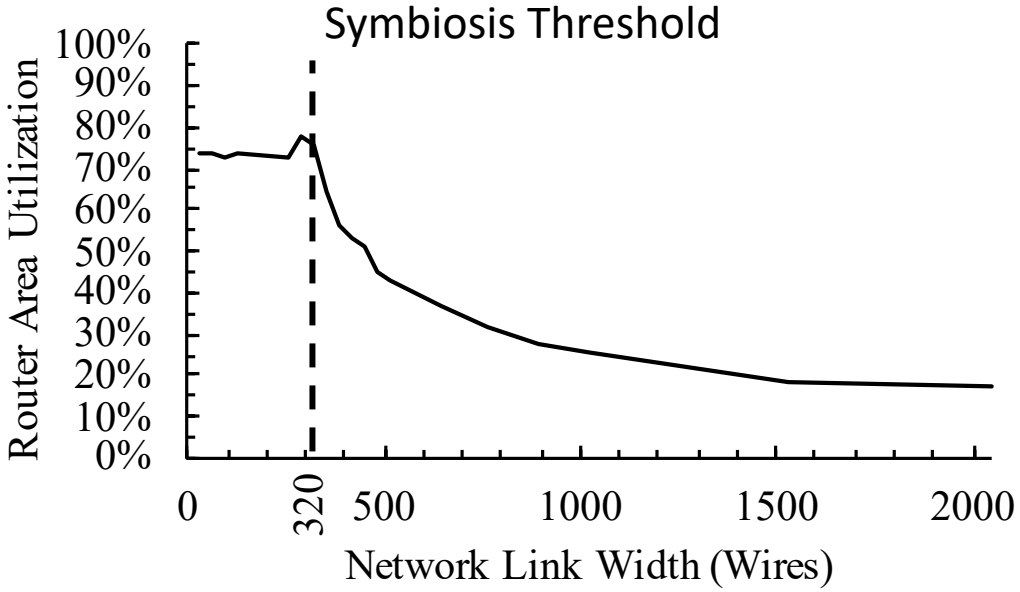
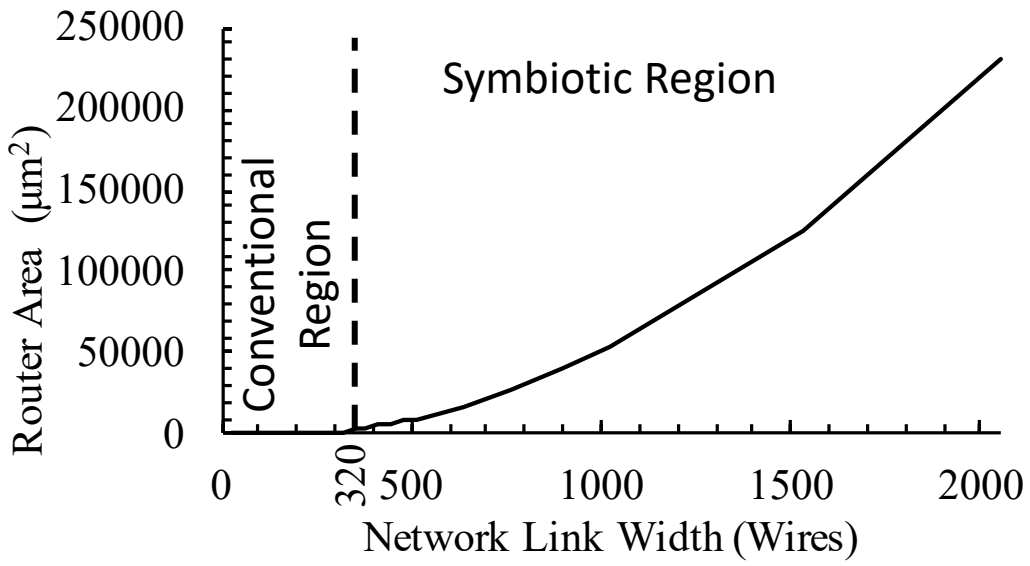


# The Threshold Separates Conventional and Symbiotic Design

**Router Area vs Link Width**

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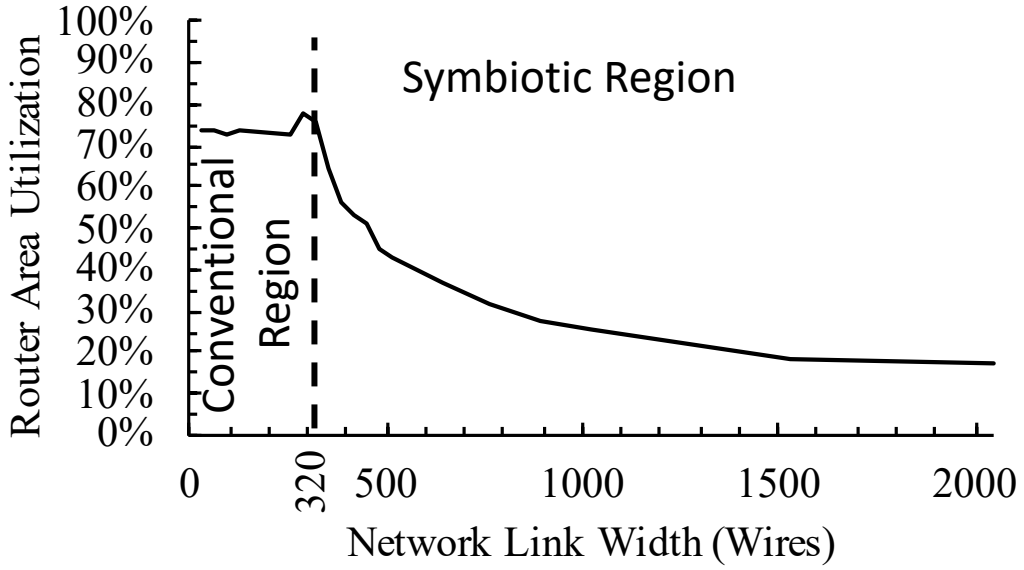
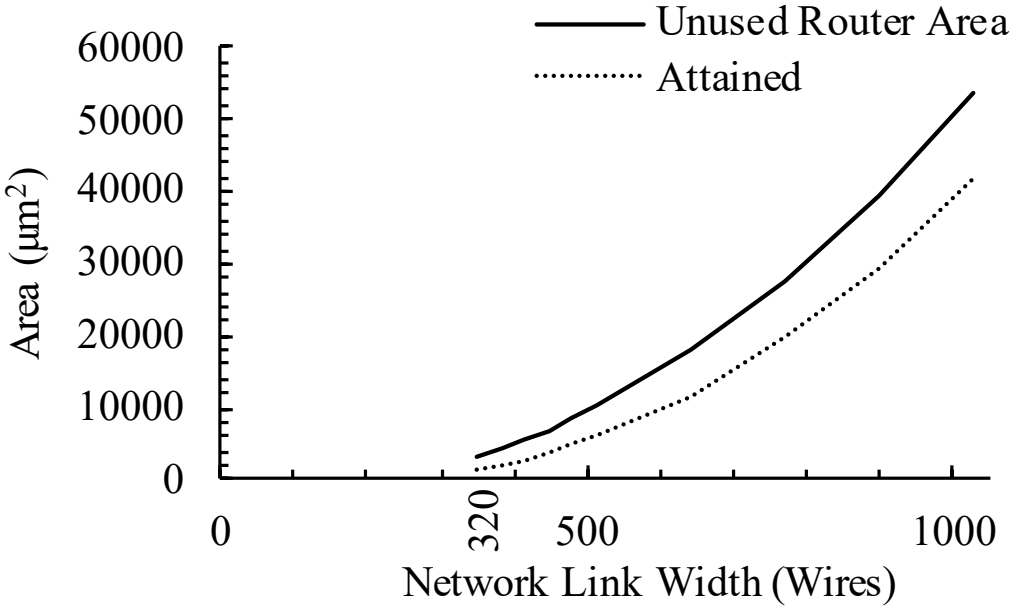
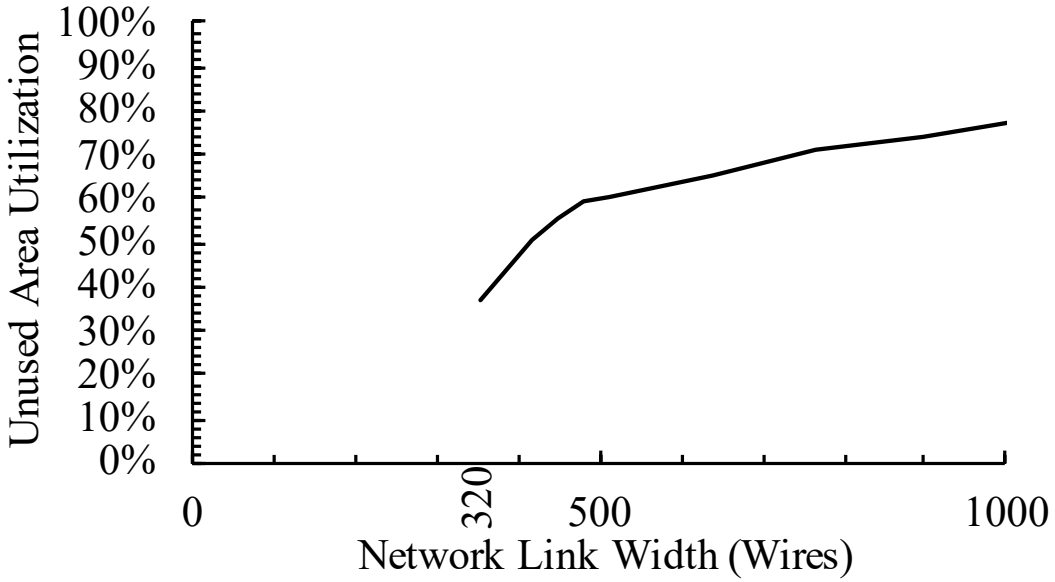


# How Effective are CAD Tools at Automatically Exploiting NoC Symbiosis?

**Recoverable Area vs Link Width**

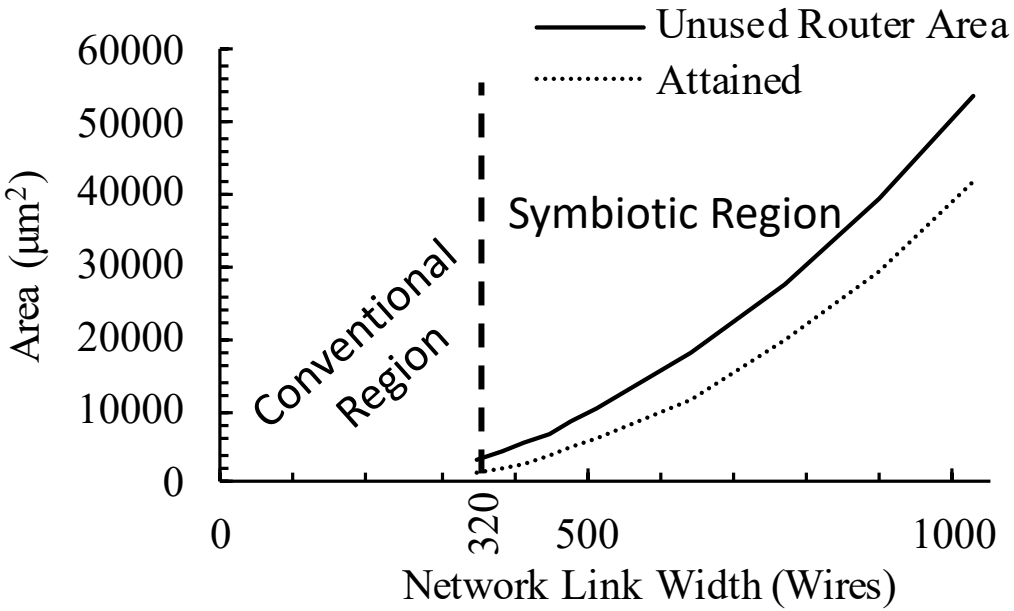



**Recoverable Utilization vs Link Width**

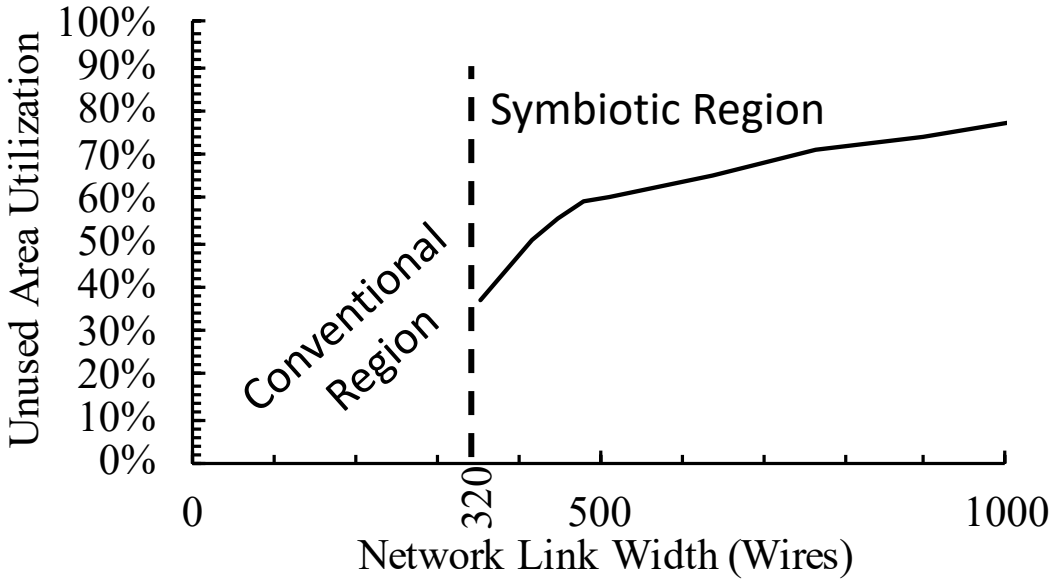


# How Effective are CAD Tools at Automatically Exploiting NoC Symbiosis?

**DLDT Recoverable Area vs Link Width**

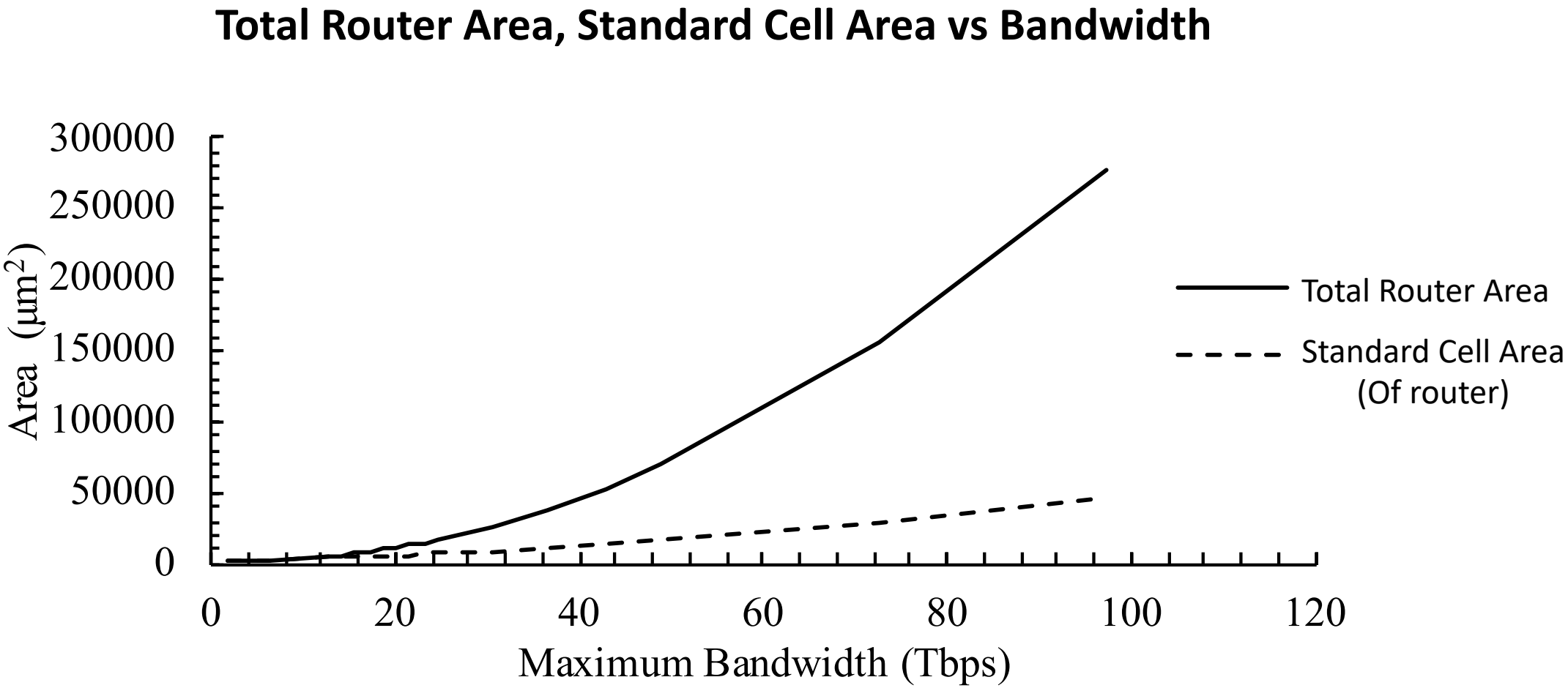



**DLDT Recoverable Utilization vs Link Width**

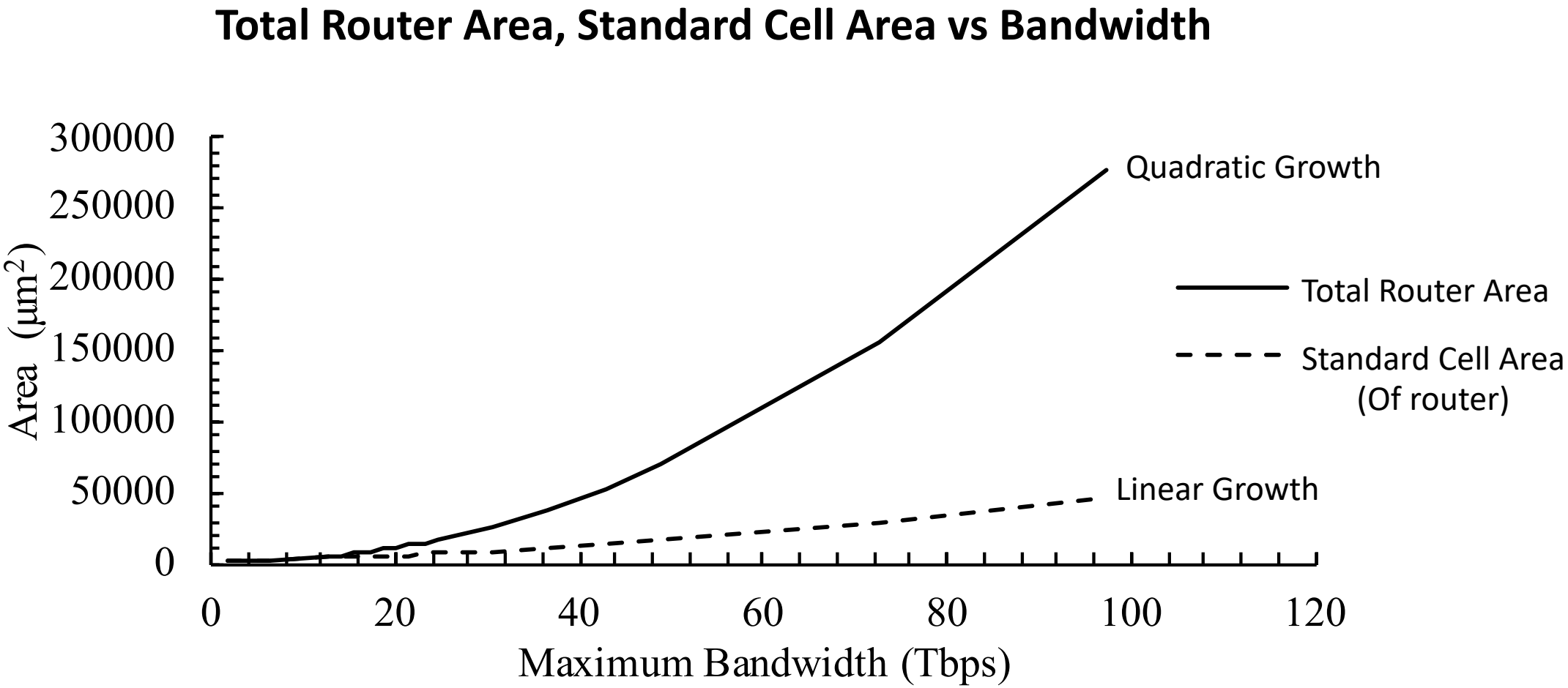



Answer: Quite effective!

# What are the Quantitative Benefits of NoC Symbiosis?



# Growth Trends Expose Bandwith/Area Trade-Off



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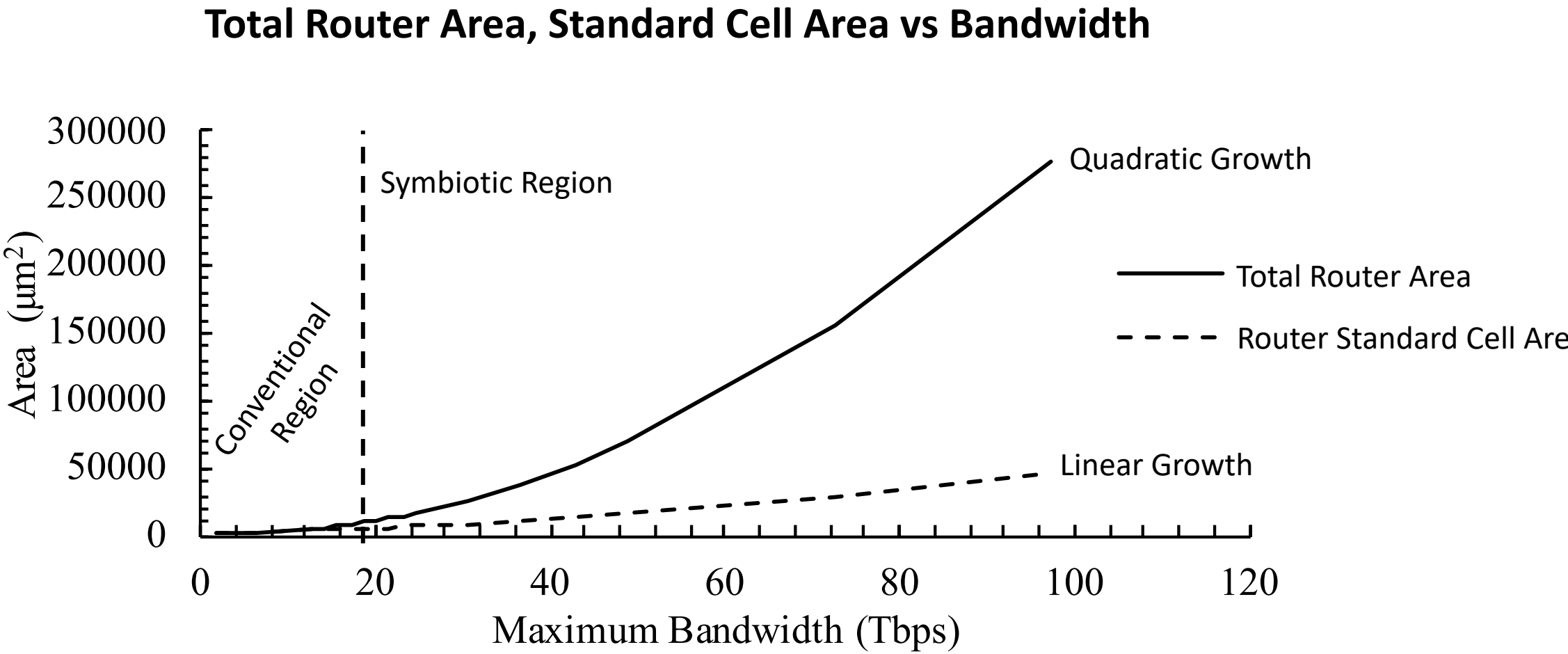
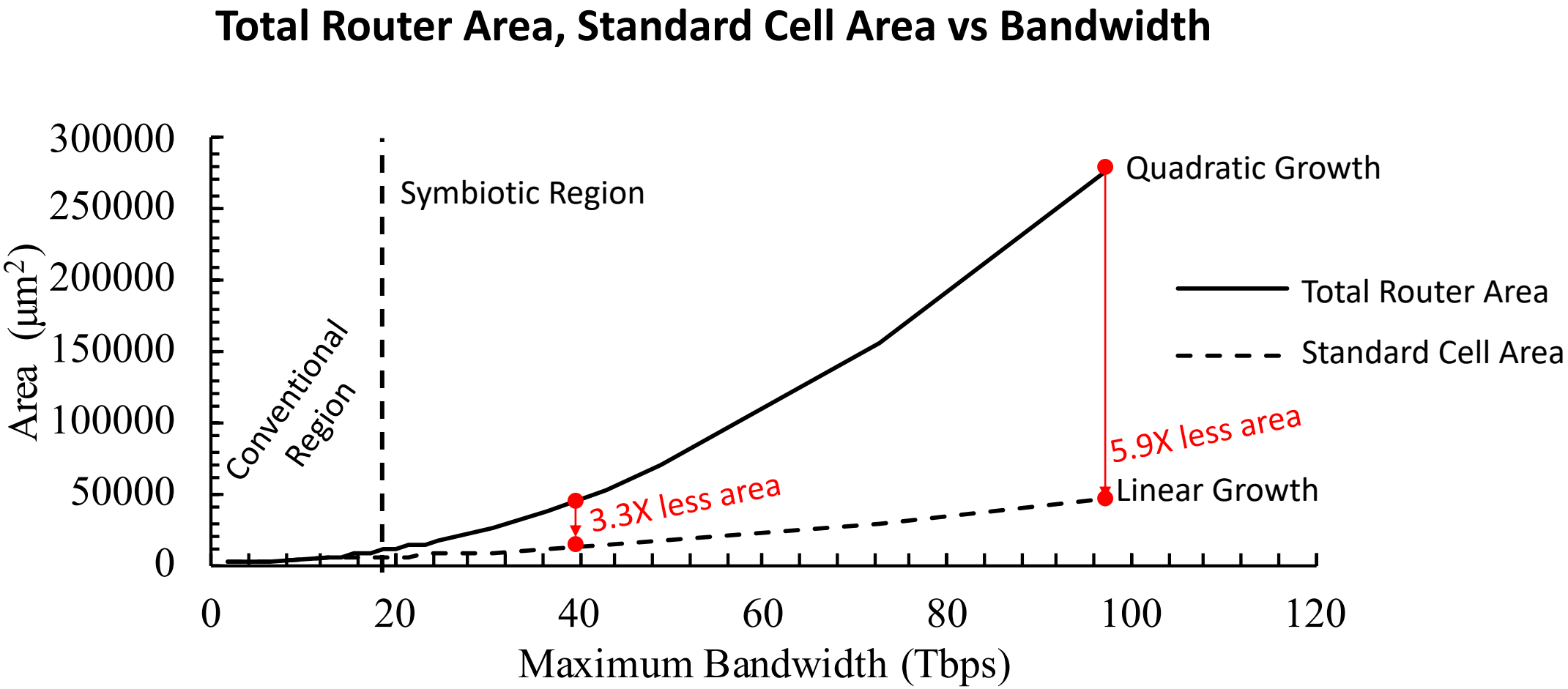


# As Your Bandwidth Needs Increase, Your Area Reduction Increases



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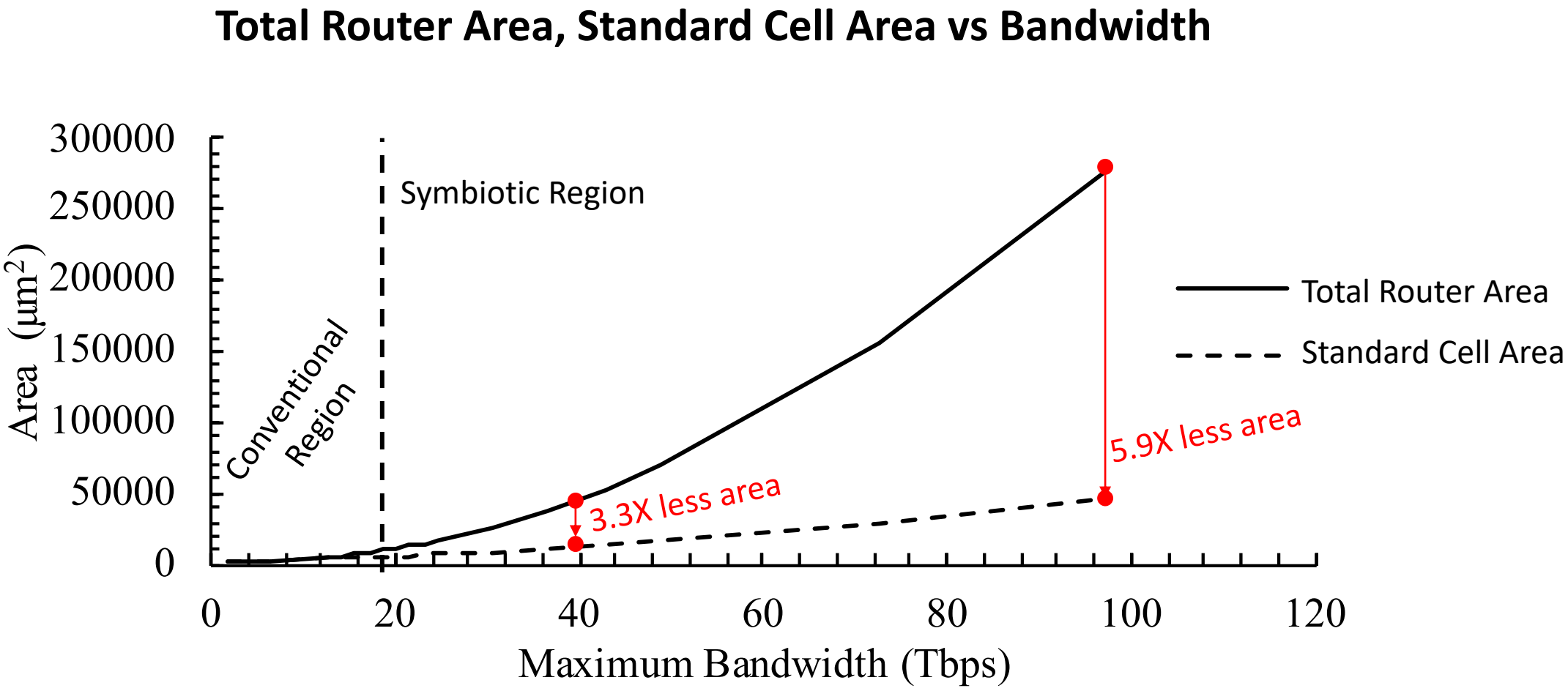
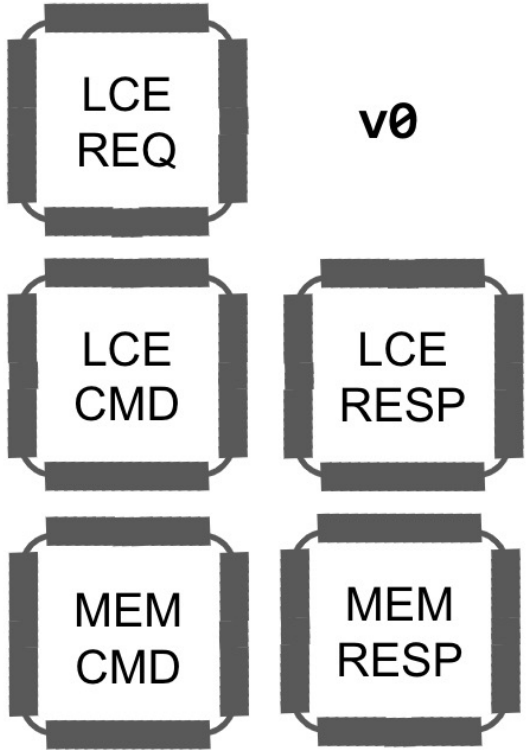



*The more bandwidth you need, the more you save!*

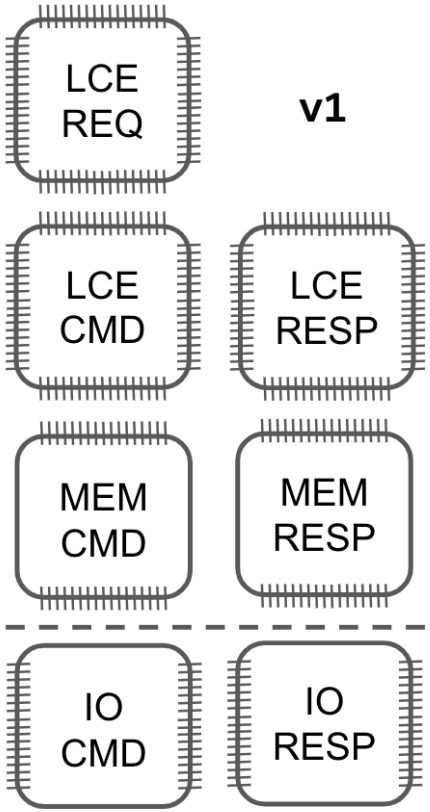
# The NoCs of Prior and Current Tiled Architectures

| | Tilera | Raw | OpenPiton | HammerBlade (HB) | EMM | BP v0 | BP v1 | BP v2 |
|---|---|---|---|---|---|---|---|---|
| **Process Node (nm)** | 90 | 180 | 32 | 12 | 45 | 40 | 12 | 12 |
| **Tile Area ($mm^2$)** | 9.6 | 16 | 1.175 | 0.025 | 0.784 | 0.832 | .360 | .360 |
| **Est. Wire Pitch (nm)** | 540 | 1080 | 192 | 128 | 270 | 240 | 128 | 128 |
| **Networks** | 5x34b | 4x34b | 3x66b | 1x56b<br>1x97b | 6x66b | 1x130b<br>2x578b<br>2x642b | 5x66b | 3x98b<br>2x130b<br>(Half-Duplex) |
| **Max Wires Per Side** | 340 | 272 | 396 | 300 | 792 | 5140 | 648 | 848 |
| **Effective Link Width** | 170 | 136 | 198 | 150 | 396 | 2570 | 324 | 424 |
| **Pin Utilization** | 5.9% | 7.3% | 7.0% | 24.3% | 24.2% | 90.2% | 13.8% | 18.1% |

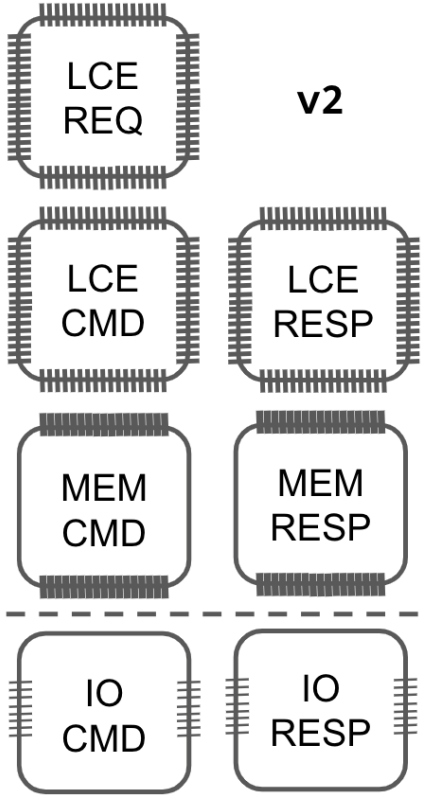
# NoC Symbiosis in Black Parrot Design Iterations




- Large networks, incredible bandwidth

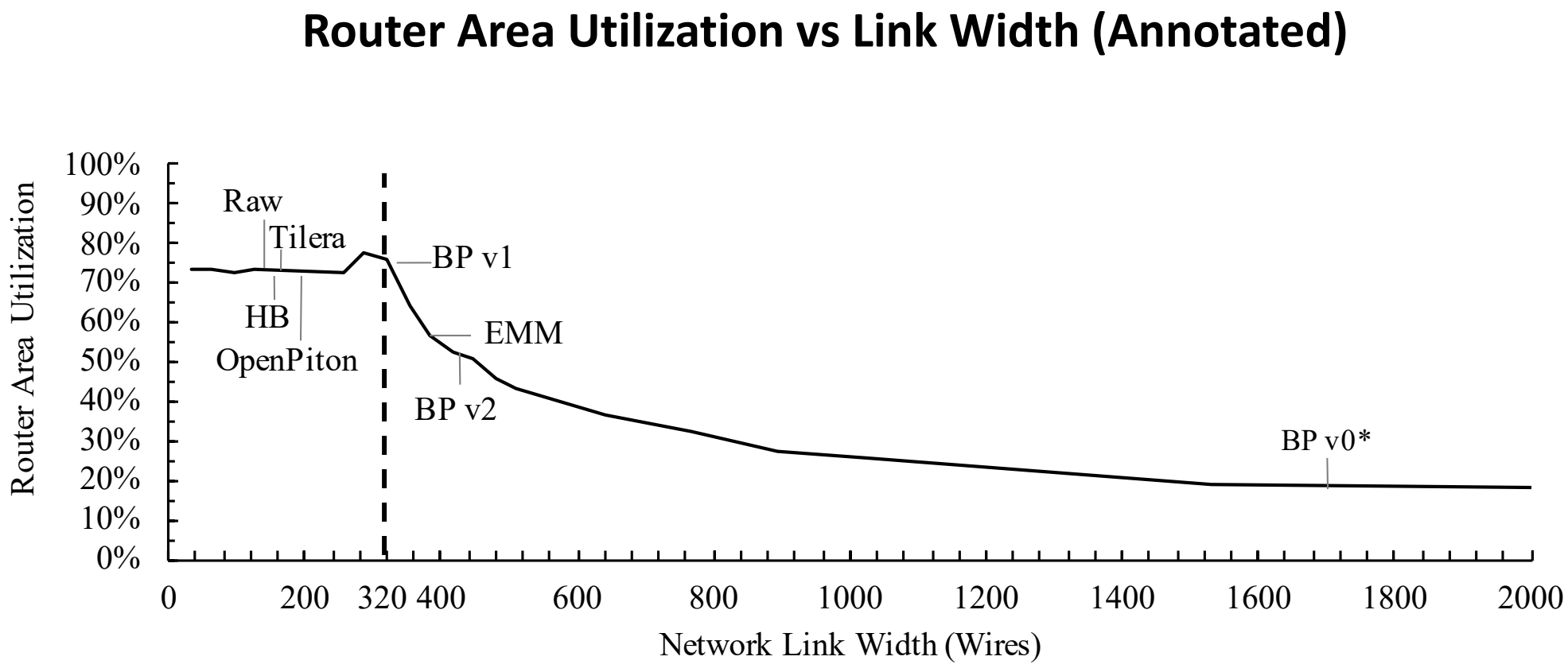



- Reduced width and dimensionality

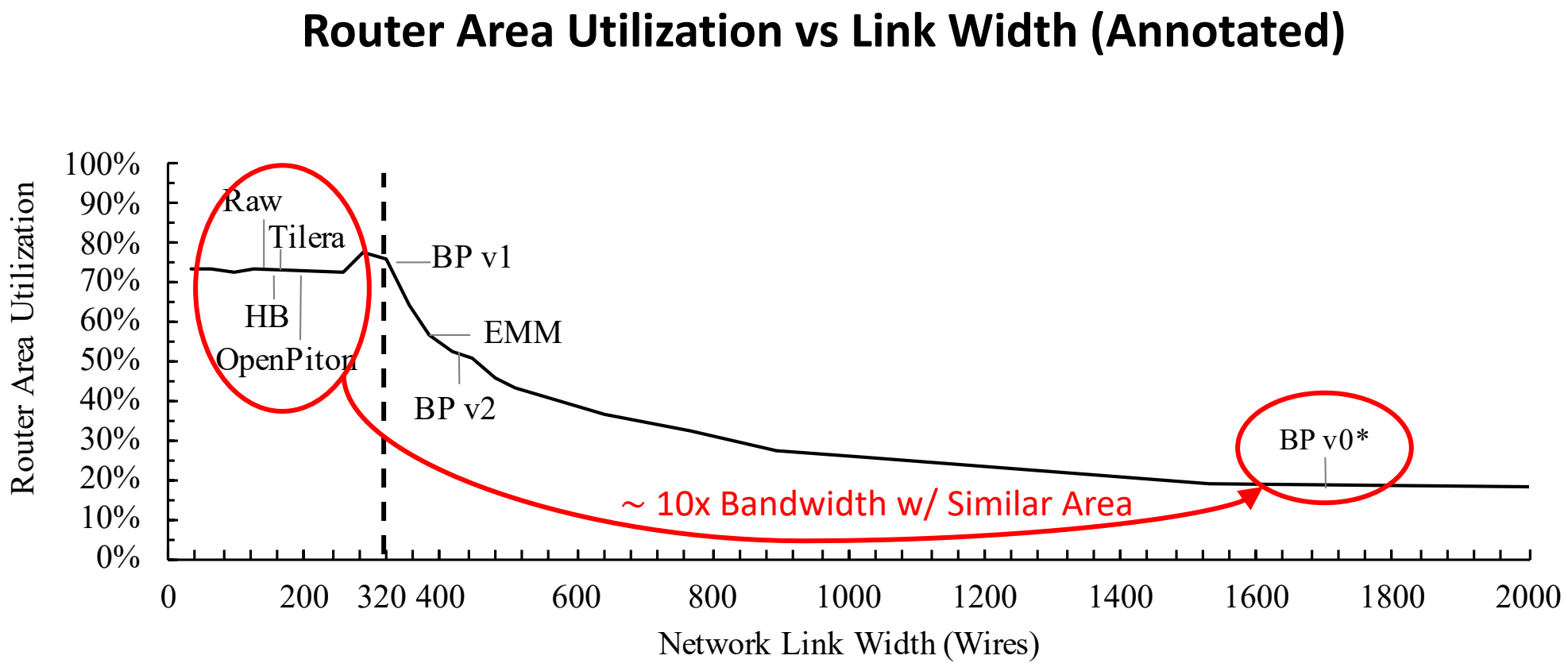



- Realistic Bandwidth Provision

# Few Designs are Symbiotic

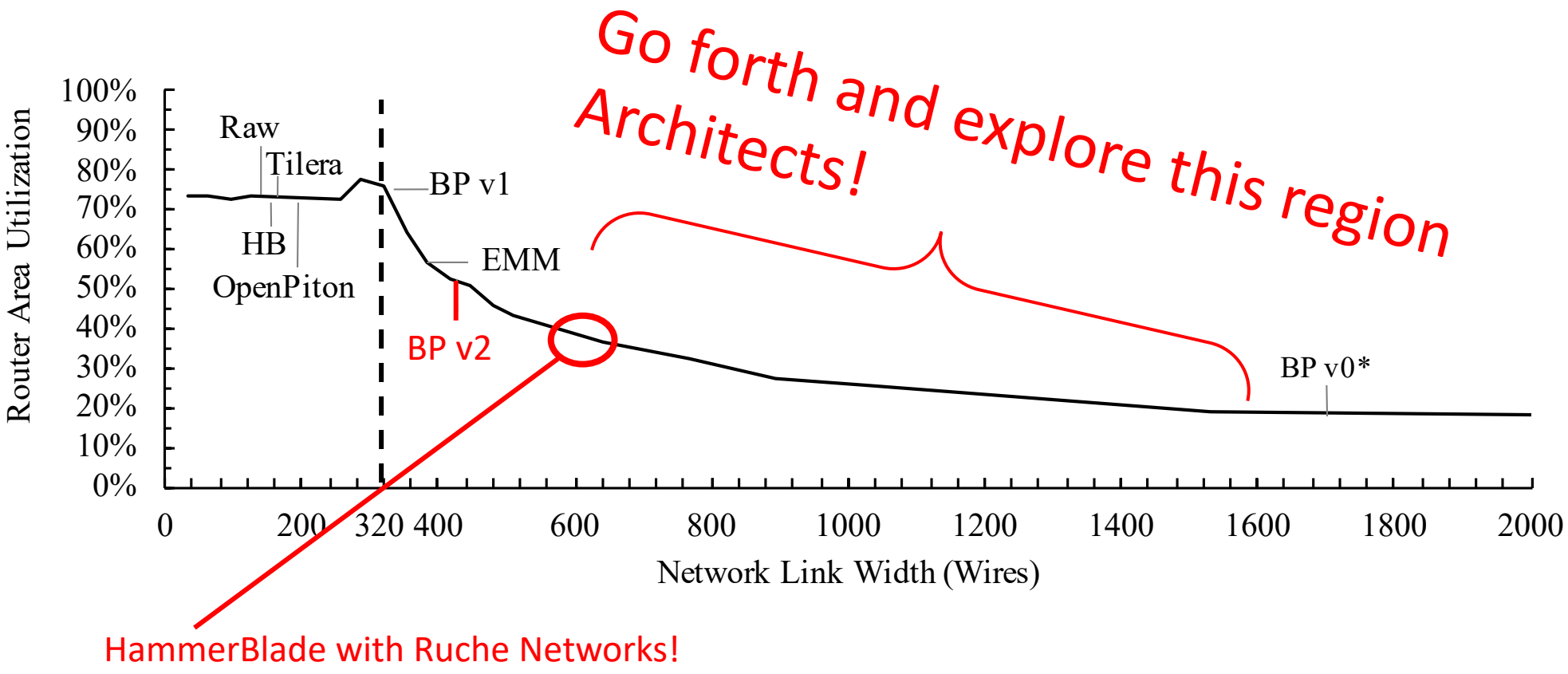


# Few Prior Designs are Symbiotic



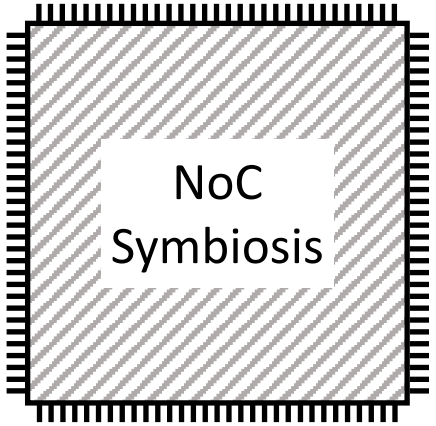
# Symbiosis Can Lead To New Architectural Possibilities

**Each architecture has a certain amount of bandwidth that it can usefully leverage and NoC Symbiosis can get you closer to the optimal point**



# NoC Symbiosis Takeaways

- Router area is under-utilized
  - *Standard Cell Area* does not increase Quadratically
- Unused area can be recovered with Symbiosis
- Area/Bandwidth Benefits
  - 8-10x Bandwidth, for small area increase
  - Smaller Routers for same Bandwidth
  - Benefits increase as network link width increases
- Few Prior Designs use NoC Symbiosis
  - But this number SHOULD increase! =)



# Acknowledgements

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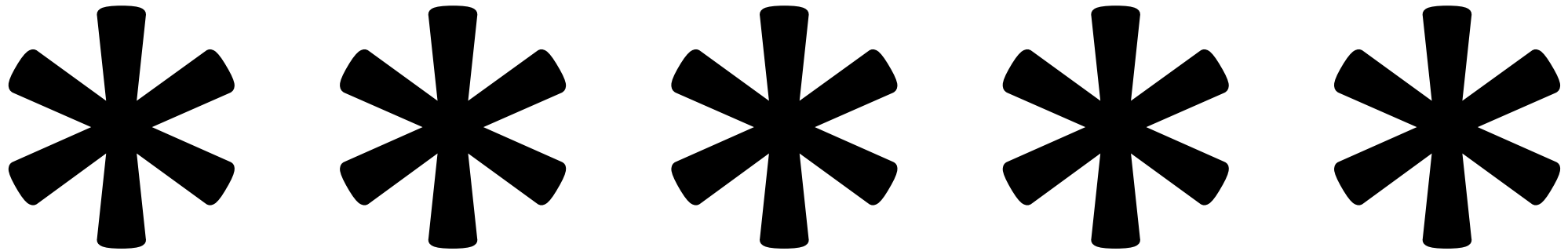
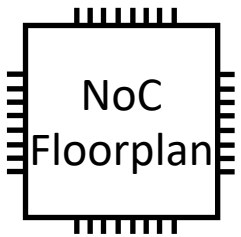
This work was partially supported by NSF SaTC Award 1563767, NSF SaTC Award 1565446, and by the DARPA/SRC JUMP ADA Center.




NoC
Floorplan